CLAIMS

What is claimed is:

1. A chip carrier for testing electrical performance of a passive component, having at least one passive component mounted on a surface of the chip carrier, the chip carrier comprising:

a core layer having a plurality of conductive traces formed on at least one surface thereof, the conductive traces comprising:

at least one first trace connected with the passive component and having a first predetermined position and two ends, wherein the two ends are respectively electrically connected to a first bond finger formed on the surface, mounted with the passive component, of the chip carrier, and to a first ball pad formed on an opposite surface of the chip carrier, and wherein the first predetermined position and the first bond finger are located on the same side relative to the passive component; and

at least one second trace free of connection with the passive component and having two ends and a second predetermined position located on the same surface as the first predetermined position, wherein one of the ends of the second trace is electrically connected to a second ball pad located on the same surface as the first ball pad; and

a solder mask layer applied over the conductive traces and formed with a plurality of openings for at least exposing the first predetermined position and the second predetermined position.

2. The chip carrier of claim 1, wherein the passive component is a resistor.
3. The chip carrier of claim 1, wherein the passive component is an inductor.
4. The chip carrier of claim 1, wherein each of the first predetermined position and the second predetermined position is at least formed with a nickel/gold (Ni/Au) layer thereon.

5. The chip carrier of claim 1, wherein the chip carrier is a substrate.
6. The chip carrier of claim 1, wherein the passive component is serially connected to the first trace by means of surface mount technology (SMT).
7. The chip carrier of claim 1, wherein the core layer is made of a material selected from the group consisting of FR4 resin, glass resin, BT (bismaleimide triazine) resin, epoxy resin, polyimide resin, and cyanide resin.
8. A method for testing electrical performance of a passive component, for use with a chip carrier having a core layer on which a plurality of conductive traces are formed, the conductive traces comprising at least one first trace predetermined to be connected with the passive component, the method comprising the steps of:

setting a first predetermined position on the first trace, and allowing two ends of the first trace to be respectively electrically connected to a first bond finger formed on a surface, mounted with the passive component, of the chip carrier, and to a first ball pad formed on an opposite surface of the chip carrier, wherein the first predetermined position and the first bond finger are located on the same side relative to the passive component;

setting a second trace from the plurality of conductive traces and a second predetermined position on the second trace, wherein the second trace is predetermined free of connection with the passive component, and one end of the second trace is connected to a second ball pad formed on the same surface as the first ball pad;

applying a solder mask layer over the conductive traces and forming a plurality of openings through the solder mask layer for at least exposing the first predetermined position and the second predetermined position;

mounting the passive component on the first trace;

interconnecting the first predetermined position and second predetermined position via an electrically conductive material; and

contacting two test heads respectively with the first ball pad and second ball pad, which are situated on the same surface of the chip carrier, to testing the electrical performance of the passive component.

9. The method of claim 8, wherein the electrically conductive material is a conductive jig made by conductive rubber.
10. The method of claim 8, wherein the electrically conductive material is a conductive jig made by a conductive metal.
11. The method of claim 8, wherein the passive component is a resistor.
12. The method of claim 8, wherein the passive component is an inductor.
13. The method of claim 8, wherein each of the first predetermined position and the second predetermined position is at least formed with a nickel/gold (Ni/Au) layer thereon.
14. The method of claim 8, wherein the chip carrier is a substrate.
15. The method of claim 8, wherein the passive component is serially connected to the first trace by means of surface mount technology (SMT).
16. The method of claim 8, wherein the core layer is made of a material selected from the group consisting of FR4 resin, glass resin, BT (bismaleimide triazine) resin, epoxy resin, polyimide resin, and cyanide resin.
17. The method of claim 8, wherein the test head is a test probe of a testing system.